



Description

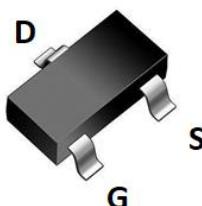
JMT P-channel Enhancement Mode Power MOSFET

Features

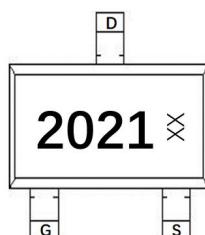
- -20V, -7A
- $R_{DS(ON)} < 24.5\text{m}\Omega$ @ $V_{GS} = -4.5\text{V}$
- $R_{DS(ON)} < 32\text{m}\Omega$ @ $V_{GS} = -2.5\text{V}$
- Advanced Trench Technology
- Provide Excellent $R_{DS(ON)}$ and Low Gate Charge
- Lead free product is acquired

Application

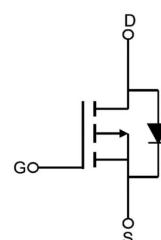
- Load Switch
- PWM Application
- Power management



SOT-23-3L top view



Marking and pin Assignment



Schematic Diagram

Package Marking and Ordering Information

Device Marking	Device	OUTLINE	Device Package	Reel Size	Reel (PCS)	Per Carton (PCS)
2021	JMTJ210P02A	TAPING	SOT-23-3L	7inch	3000	120000

Absolute Maximum Ratings ($T_A=25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter		Max.	Units
V_{DSS}	Drain-Source Voltage		-20	V
V_{GSS}	Gate-Source Voltage		± 12	V
I_D	Continuous Drain Current	$T_A = 25^\circ\text{C}$	-7	A
		$T_A = 100^\circ\text{C}$	-4.6	A
I_{DM}	Pulsed Drain Current ^{note1}		-28	A
P_D	Power Dissipation	$T_A = 25^\circ\text{C}$	2	W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient		62.5	$^\circ\text{C}/\text{W}$
T_J, T_{STG}	Operating and Storage Temperature Range		-55 to +150	$^\circ\text{C}$

**Electrical Characteristics** ($T_J=25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
Off Characteristic						
$V_{(\text{BR})\text{DSS}}$	Drain-Source Breakdown Voltage	$V_{GS}=0\text{V}$, $I_D = -250\mu\text{A}$	-20	-	-	V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = -20\text{V}$, $V_{GS}=0\text{V}$,	-	-	-1	μA
I_{GSS}	Gate to Body Leakage Current	$V_{DS}=0\text{V}$, $V_{GS}= \pm 12\text{V}$	-	-	± 100	nA
On Characteristics						
$V_{GS(\text{th})}$	Gate Threshold Voltage	$V_{DS}=V_{GS}$, $I_D = -250\mu\text{A}$	-0.4	-0.7	-1.0	V
$R_{DS(\text{on})}$ note2	Static Drain-Source on-Resistance	$V_{GS} = -4.5\text{V}$, $I_D = -7\text{A}$	-	18.7	24.5	$\text{m}\Omega$
		$V_{GS} = -2.5\text{V}$, $I_D = -5\text{A}$	-	22.7	32	
Dynamic Characteristics						
C_{iss}	Input Capacitance	$V_{DS} = -10\text{V}$, $V_{GS}=0\text{V}$, $f=1.0\text{MHz}$	-	2000	-	pF
C_{oss}	Output Capacitance		-	242	-	pF
C_{rss}	Reverse Transfer Capacitance		-	231	-	pF
Q_g	Total Gate Charge	$V_{DS} = -10\text{V}$, $I_D = -3\text{A}$, $V_{GS} = -4.5\text{V}$	-	15.3	-	nC
Q_{gs}	Gate-Source Charge		-	2.2	-	nC
Q_{gd}	Gate-Drain("Miller") Charge		-	4.4	-	nC
Switching Characteristics						
$t_{d(on)}$	Turn-on Delay Time	$V_{DD} = -10\text{V}$, $I_D = -7\text{A}$, $V_{GS} = -4.5\text{V}$, $R_{\text{GEN}} = 2.5\Omega$	-	10	-	ns
t_r	Turn-on Rise Time		-	31	-	ns
$t_{d(off)}$	Turn-off Delay Time		-	28	-	ns
t_f	Turn-off Fall Time		-	8	-	ns
Drain-Source Diode Characteristics and Maximum Ratings						
I_s	Maximum Continuous Drain to Source Diode Forward Current	-	-	-7	A	
I_{SM}	Maximum Pulsed Drain to Source Diode Forward Current	-	-	-28	A	
V_{SD}	Drain to Source Diode Forward Voltage	$V_{GS}=0\text{V}$, $I_s = -7\text{A}$	-	-0.8	-1.2	V

Notes:1. Repetitive Rating: Pulse Width Limited by Maximum Junction Temperature

2. Pulse Test: Pulse Width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$

Typical Performance Characteristics

Figure 1: Output Characteristics

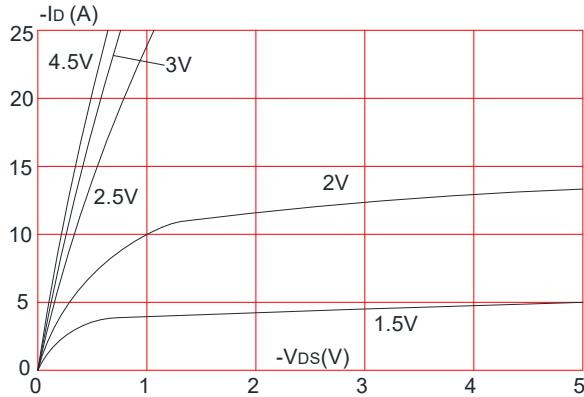


Figure 3: On-resistance vs. Drain Current

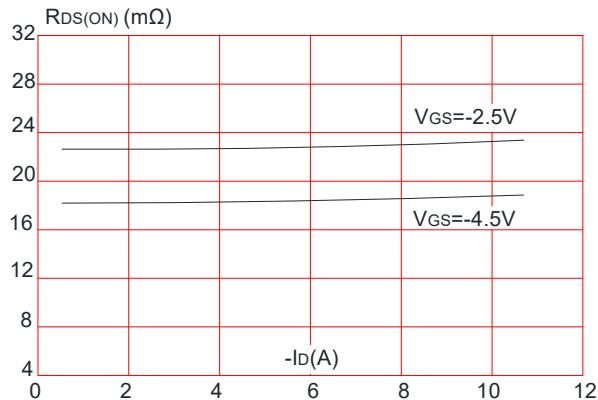


Figure 5: Gate Charge Characteristics

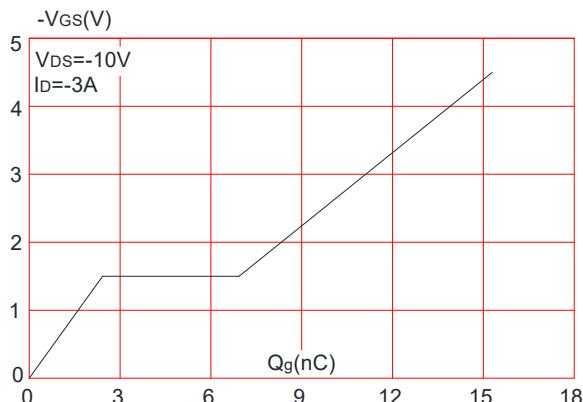


Figure 2: Typical Transfer Characteristics

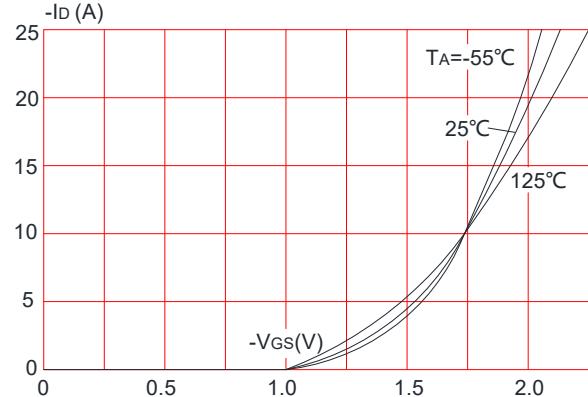


Figure 4: Body Diode Characteristics

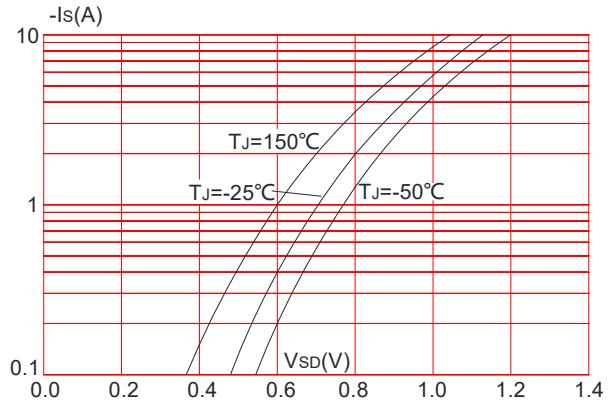


Figure 6: Capacitance Characteristics

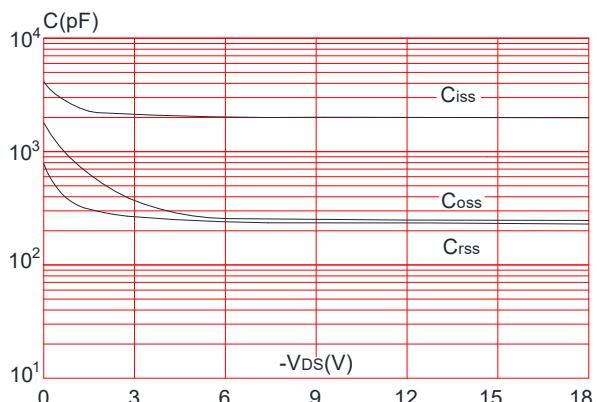


Figure 7: Normalized Breakdown Voltage vs. Junction Temperature

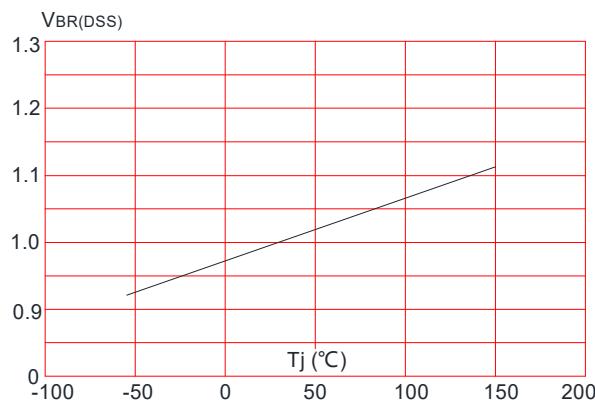


Figure 8: Normalized on Resistance vs. Junction Temperature

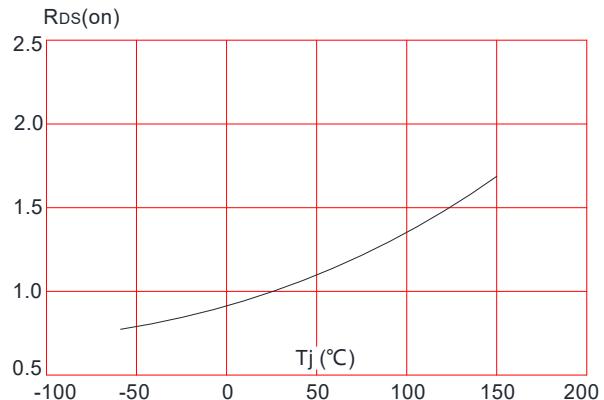


Figure 9: Maximum Safe Operating Area

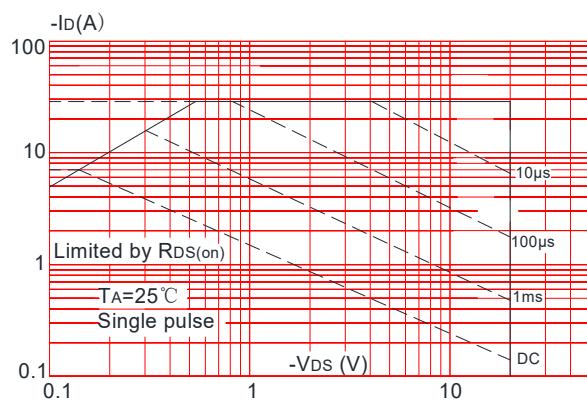


Figure 10: Maximum Continuous Drain Current vs. Ambient Temperature

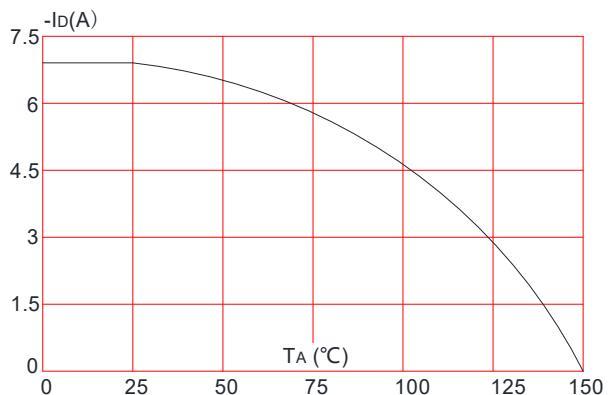
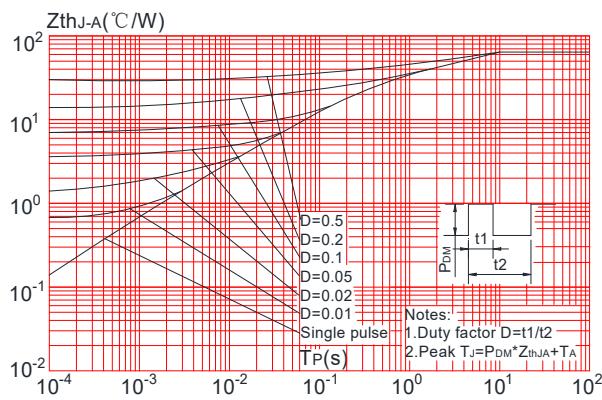
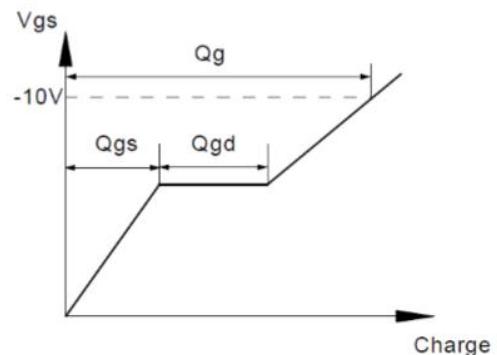
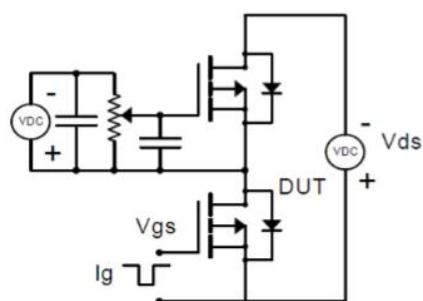


Figure 11: Maximum Effective Transient Thermal Impedance, Junction-to-Ambient

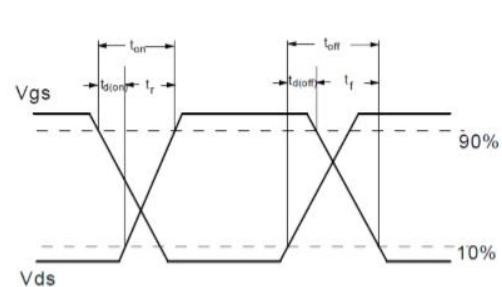
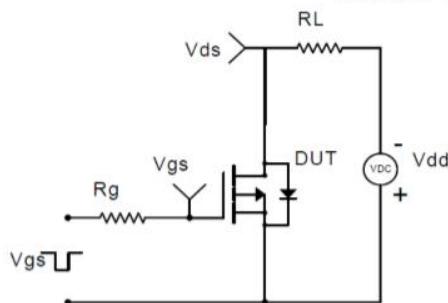


Test Circuit

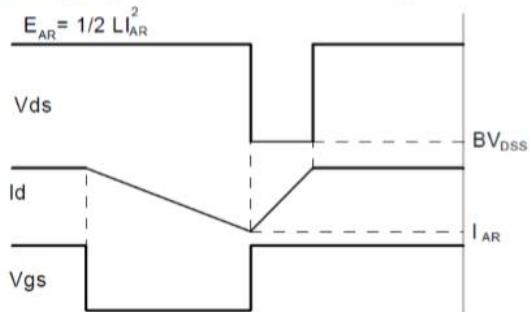
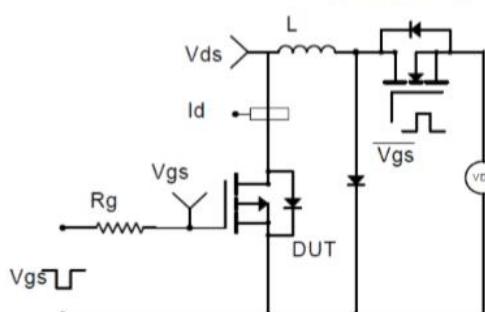
Gate Charge Test Circuit & Waveform



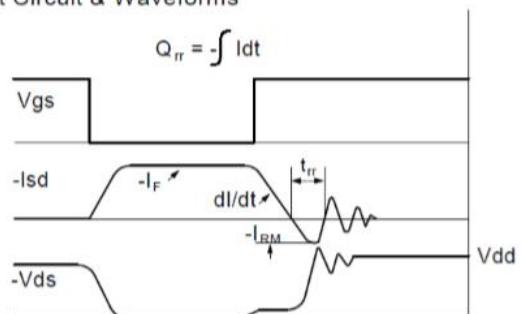
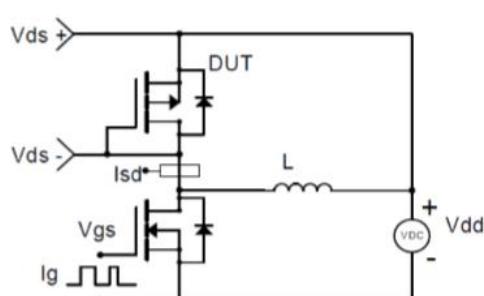
Resistive Switching Test Circuit & Waveforms



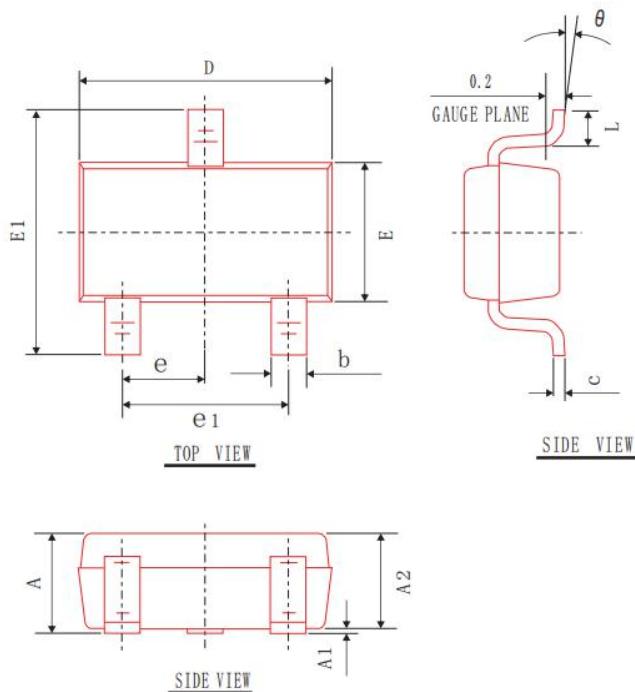
Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms



Package Mechanical Data- SOT-23-3L

COMMON DIMENSIONS
(UNITS OF MEASURE=mm)

SYMBOL	MIN	NOM	MAX
A	—	—	1.30
A1	0.00	0.05	0.10
A2	1.00	1.10	1.20
b	0.30	0.40	0.50
c	0.119	0.127	0.135
e1	1.80	1.90	2.00
D	2.80	2.90	3.00
E	1.50	1.60	1.70
E1	2.60	2.80	3.00
L	0.30	0.45	0.60
θ	0°	4°	8°
e	0.95BSC		

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